Drawing Package Supplement to

ASTERoids DELUXE™

CABARET

Operation, Maintenance and Service Manual

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REGULATOR/AUDIO I PCB SCHEMAIC (034485-03 A)

Regulator/Audio I PCB

The Regulator/Audio I PCB has the dual functions of regulating the +5 VDC logic power to the game PCB and amplifying the audio from the game PCB.

Regulator Circuit

The regulator consists of voltage regulator Q1, current source power transistor Q3 and Q3's bias transistor Q2. The regulator accurately regulates the logic power input to the game PCB by monitoring the voltage through high-impedance inputs +SENSE and -SENSE. The inputs are directly from the +5 VDC and ground inputs to the game PCB. Therefore, the regulator regulates the voltage on the game PCB. This eliminates a reduced voltage due to IR drop up the wire harness between the regulator and the game PCB. Variable resistor R8 is adjusted for the +5 VDC on the game PCB. Once adjusted, the voltage at the input of the game PCB will remain constant at this voltage.

Regulator Adjustment

1. Connect a voltmeter between +5 V and GND test points of the game PCB.
2. Adjust variable resistor R8 on the Regulator/Audio I PCB for +5 VDC reading on the voltmeter.
3. Connect a voltmeter between +5 V REG and GND on the Regulator/Audio I PCB. Voltage reading must not be greater than +5.5 VDC. If greater, try cleaning edge connectors on both the game PCB and the Regulator/Audio I PCB.
4. If cleaning PCB edge connectors doesn't decrease voltage difference, connect minus lead of voltmeter to GND test point of Regulator/Audio I PCB and plus lead to +5 V REG test point on Regulator/Audio I PCB. Now connect minus lead of voltmeter to +5 REG test point on game PCB. From this you can see which harness circuit is dropping the voltage. Troubleshoot the appropriate harness wire or harness connector.

Audio Circuit

The audio circuit contains two independent audio amplifiers. Each amplifier consists of one 70690024 amplifier with a gain of ten.

AMERICAN-MADE COIN DOOR SCHEMATIC (034988-01 A)

BRITISH-MADE COIN DOOR SCHEMATIC (037050-01 A)
**CLOCK CIRCUIT**

The clock circuit consists of crystal Y1 and associated inverters and counters C3 and B3. Counters C3 and B3 count the crystal frequency, down to the frequencies necessary for the Asteroids Deluxe™ game.

**NOTE:**
The MPU chip used in the game operates at a frequency of 1.5 MHz. Therefore, the MPU chip must be the 6502A. The 6502A's maximum frequency is 1 MHz and is not compatible with this game.

**POWER RESET AND WATCHDOG COUNTER**

During initial power-up, the delayed charging of capacitor C22 causes a preset of flip-flop C3 and a clear of counter D4. This results in holding the reset input to the low. When the charge of C22 reaches about 1.5 VDC, preset and clear inputs are removed. Counter D4 counts to 128 at 3 kHz rate, and reset is removed (goes high) from the input of the MPU. This allows the logic power input to the PCB to stabilize before allowing the MPU to begin its initialization routine.

If the MPU program is operating properly, the MPU address decoding circuitry will output the WDKR (Watchdog clear) signal at predetermined intervals. This serves to clear counter D4 before it counts up to the state that will cause the reset condition. If the MPU program stays from its intended sequence and does not output the WDKR signal, counter D4 will count up to the reset state and cause the MPU to return to its initialization routine.

Denotes a change by indicated revision

Denotes a test point

**NMI COUNTER**

The NMI (non-maskable interrupt) counter causes an interrupt at the NMI input of the MPU every 4 nsec. The interrupt is derived by dividing 3 MHz by a factor of 12 through counter C4. The interrupt occurs when pin 5 of inverter B4 goes low. During power-up, the NMI counter is disabled by reset. During self-test, the NMI is disabled by TEST.

**POWER INPUT**

This circuity consists of the PCB inputs and outputs for the +5 VDC logic and 25 VAC input to the on-board regulators. The +5 VDC inputs and outputs are discussed on Sheet 1, Side A of this schematic set.

The 25-VAC inputs are received by two full wave rectifiers. Diodes CR1 and CR2 rectify the negative cycle of the input and the 796 regulates the voltage at +5 VDC. Diodes CR3 and CR4 rectify the positive pulse of the 25 VAC input and the 7805 regulates the voltage at +5 VDC. The 7812 regulates at +12 VDC. The 7805 regulates an additional 5 VDC for the DACs. Zone diode CR5 supplies the +8.3 VDC for the sample and hold circuit. The +22 VDC unregulated is used to power operational amplifiers P1 and L8 in the audio output.

Denotes a test point

**ROM/PROM CIRCUITRY**

Program memory for the Asteroids Deluxe™ game is contained in three ROMs.

**RAM CIRCUITRY**

The RAM is the temporary memory of the MPU and is enabled when Page enable is low. When Page enable is low, the RAM strobe (DB9 thru DB0) is active. By the MPU address bus, the RAM reads a byte at the addressed location.

The signal RAMSEL reflects the state of the Page enable on the RAM, which allows greater flexibility.
The state machine is the “master controller” of the vector-generating circuitry. It receives instructions from the game MPU, via the vector generator RAM. It carries out these instructions by accessing the appropriate sections of the vector-generate ROM memory, using the vector-generator program counter to do so. The state machine reads the vector-generator ROM data (via RAM) and decodes this information to determine how it should be used: 1) to draw a vector, 2) to move the monitor beam to a new position on the monitor display, 3) to “jump” to a new vector memory address, 4) to return to a previous vector memory address, 5) or to tell the game MPU that it has completed its current instructions, and is waiting for its next command.

The state machine consists of input gates B1 and E5, ROM C6, latch D8, clock circuitry A6, and decoder E8. Four-bit input TIMERS thru TIMERS is the operation-code input to the state machine. The A4 thru A6 address bus from ROM C8 tells the ROM which instructions to perform. Address inputs A0 thru A3 from latch D8 tell the ROM which state was last performed. The address A7 input G0 tells the ROM if the position counters are presently drawing a vector. The HALT input to A7 tells the ROM that the vector generator has completed its operations.

During initial power-up of the game, the HALT signal is present low. The microcomputer reads the high HALT signal through its switch input port (signal U130) on data line D7. This tells the microcomputer that the vector generator is halted and waiting for an instruction. To ensure that the beam is off when the state machine is halted, the high HALT clocked through latch D8, results in a low BLANK to the Visible axis output.

The microcomputer outputs an address that results in a D630 read signal that causes the RAM to go high, and clears the vector-generator data latches. This makes the microcomputer 1024 signals all low. The state machine now begins executing instructions, starting at vector memory location 0.

When the state machine receives the operation code for a HALT instruction, it outputs a low HALTROST, setting the HALT flip-flop A8, and suspending state machine operation.

The GO signals load and enable the vector timer and the X and Y position counters and tell the ROM that the vector generator is now actively drawing a vector. The HALT input to GO flip-flop A3 sets the outputs to ensure that the vector timer and position counters are not active. The state machine is halted. When a low GOstrobe is clocked through A8, the vector timer and X and Y position counters begin to operate from GO, GO strobe, and GO strobe signals. When GO strobe is clocked through A8, the vector timer has reached its maximum count, and GO goes high. This means the vector has been drawn.

The VGOK input to the clock circuit is a buffered 1.5-MHZ clock signal from the microcomputer. This is the same frequency used to clock the MPU of the microcomputer. The signal clocks latch D8 unless the microcomputer is addressing the vector RAM or ROM memories (where VMEM goes low). Then the clock input to latch D8 goes high and stays high until VMEM goes high.

The purpose of the vector timer is to time out the length of time it takes to “draw” an actual vector on the monitor display. During the interval when the X- and Y-position counters are actually writing the vector, STOP is high. This prevents the vector-generator state machine from advancing to its next state until the vector actually being drawn is completed. As soon as the vector has been drawn, STOP goes low, allowing the state machine to advance to the next state in its intended sequence.

The vector timer consists of multiplexer F5, decoder E8, latch M8, adder M5, and counters B6, C6, and D6. M5 contains a scale factor which is added to M5 for the four timer signals. If TIMERO thru TIMERO inputs are any state but all high, decoder E8 directly decodes the sum and loads the decoded value into one of the count-ers. When GO goes low, the counters count from the loaded count to the counter reach their maximum count. This count is a maximum length of 1024. At this time STOP goes low and clears the GO flip-flop of the state machine.

If the TIMER signals are all high, APOPHANOS goes low and data signals D9 and D9 are decoded by decoder E8. This is added to the scale factor and loaded into the counters.
DIAG STEP (diagnostic step), 3 KHz, SELF-TEST SLAM, HALT, FIRE, and SHIELD switches are read by the MPU when SINP= (switch input pin enabled) is low. Switches to be read are selected by A80 thru A82 from the MPU. All inputs are read on DB7. Switch inputs are active when pulled to ground. DIAG STEP, 3 KHz, and SELF-TEST are signals read by the MPU to initiate and control the game's self-test procedure. SLAM is a signal read by the MPU to indicate the status of the anti-sneak switch mounted on the coin door. The MPU reads HALT to determine the state of the vector generator.

The coin door and some control panel switches are read by the MPU when SINP= (switch input pin enabled) is low. Switches to be read are selected by A80 thru A82 from the MPU. All inputs are read on data line DB7. Switch inputs are "on" when pulled to ground.

The game option switches are read by the MPU when OPCS option switch enabled is low. Switch toggles to be read are selected by A80 and A81 from the MPU. Switch toggles 1, 3, 5 and 7 are read on data line DB8 and toggles 2, 4, 6, and 8 are read on DB1. Toggle inputs are "on" when pulled to ground.

The + and y-video inverter circuits are identical; therefore, only the x-video inverter circuit is explained. For inverted video operation, pin 19 is grounded which turns on transistor Q13 and turns off transistor Q12. In this state INV is +.2 VDC and NONINV is .2 VDC.

For a noninverted video output, pin 19 is unconnected and floats. In video games, pins 19 and 7 are shorted and have a potential of +5 VDC. This causes transistor Q13 to be cut off and transistor Q12 to be turned on. INV is then -.2 VDC and NONINV is approximately +.2 VDC.

In upright games, only the x-video inverter is used. In cocktail games both x and y-video inverters are used, and in cabinet games the x-video inversion is not necessary, so neither is used.

The EXPLODE sound is heard when any object explodes. Noise is shaped at a frequency determined by P7, and control bits EXPITCH and EXPITCH. Changing the shaping rate changes the pitch of the explosion. The noise is amplified modulated in R6 by EXPAUD EXPAUD.

R7 and R8 generate random noise. This noise is filtered by P11 and produces the rumble sound heard when the ship is thrusting.
The video-output circuit consists of three individual circuits: X-axis, Y-axis, and Z-axis. The X-axis and Y-axis video-output circuits each consist of a digital-to-analog converter (DAC), current-to-voltage converter, two sample and hold, and amplifier. The Z-axis video-output circuit consists of a shift register and a summer.

**X and Y Outputs**

The DACs D11 and B11 each receive binary numbers from the vector generator's position counter outputs. These numbers represent the location of the beam on the monitor. For the non-inverted X-axis, the numbers range from 0 to 1023, where 0 is at the far left of the monitor screen, 512 is at the center, and 1023 is at the far right. For the non-inverted Y-axis, the numbers range from 128 to 998, where 128 is at the bottom of the monitor screen, 512 is at the center, and 998 is at the top. When the X-axis and Y-axis are inverted, the monitor picture is turned upside down. This is used for a two-player cocktail game.

The DACs convert these binary number inputs to current outputs. The DACs current outputs are applied to the pin 6 inputs of current-to-voltage converters C12 and A12.

From the current-to-voltage converters, the signal is fed to two sample-and-hold circuits. One is non-inverted and the other is inverted. The non-inverted sample and hold consists of one stage of analog switch D12 and capacitor C98 for the X-axis and B12 and C99 for the Y-axis. The inverting sample and hold consists of inverter E12, one stage of analog switch D12, and capacitor C98 for the X-axis and B12/C12/B10/C10 for the Y-axis.

The sample-and-hold circuits are controlled by SHCON (sample and hold control). SHCON is derived by gating 3 MHz from the microcomputer clock and VDGX from the vector generator's state generator. The result of these inputs is that the non-inverted and inverted analog signals that are applied to the analog switches have sufficiently stabilized before being applied to the sample-and-hold capacitors.

The output swing of SHCON is 8 to +8 VDC. When SHCON is high, the voltage charge of the sample-and-hold capacitors to the X and Y analog voltage value. The voltages are then applied to the inputs of the second analog switch. These switches select either the non-inverted or inverted X and Y axes outputs. The outputs are then amplified by the second stages of C12 and A12 for an impedance-matched output to the X and Y inputs to the monitor. Since the monitor doesn't have field-adjustable X and Y gains, the gains are adjustable by variable resistors R120 and R126.

**Z Output**

The Z-axis video output receives six inputs. BVLD (beam valid), from the output of the vector generator's position counters, tells the Z-axis to draw the lines. BLK (black) from the vector generator's state machine, tells the Z-axis to stop drawing a line. SCALLED (scaled) from the output of the vector generator's data clock, tells the Z-axis the grey-scale shading of the line that is being drawn on the monitor.

When BVLD and BLK are both high, a high is clocked through the shift register R9 that turns transistor Q3 off. This allows the scale inputs to be passed through transistor Q2. When BLK goes low, a low is clocked through R9, transistor Q3 turns on, and the signal is grounded at the base of transistor Q2.

The scale inputs at the base of transistor Q1 determine Q1's emitter voltage, during the line draw period. The SCALLED thru SCALE3 resistors R96 thru R36, resistor R36, and resistor R40 result in a range of about +1.0 VDC when all are low and +4.0 VDC when all are high. The emitter of transistor Q1 follows at about +1.7 to +4.7 VDC, while the emitter of transistor Q2 follows at about +1.0 to +4.0 VDC. This output is applied to the Z input of the monitor. Since there are brightness and contrast controls in the monitor, there are no adjustments in this circuit.